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Smayling

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(54) **SUPER-SELF-ALIGNED CONTACTS AND METHOD FOR MAKING THE SAME**

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(57)   **ABSTRACT**

A number of first hard mask portions are formed on a dielectric layer to vertically shadow a respective one of a number of underlying gate structures. A number of second hard mask filaments are formed adjacent to each side surface of each first hard mask portion. A width of each second hard mask filament is set to define an active area contact-to-gate structure spacing. A first passage is etched between facing exposed side surfaces of a given pair of neighboring second hard mask filaments and through a depth of the semiconductor wafer to an active area. A second passage is etched through a given first hard mask portion and through a depth of the semiconductor wafer to a top surface of the underlying gate structure. An electrically conductive material is deposited within both the first and second passages to respectively form an active area contact and a gate contact.

20 Claims, 32 Drawing Sheets
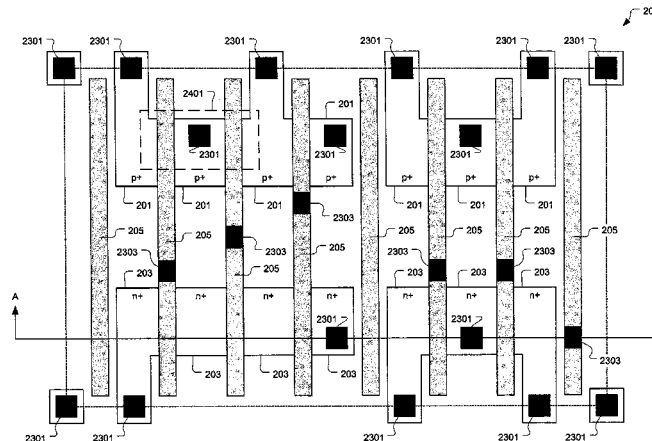
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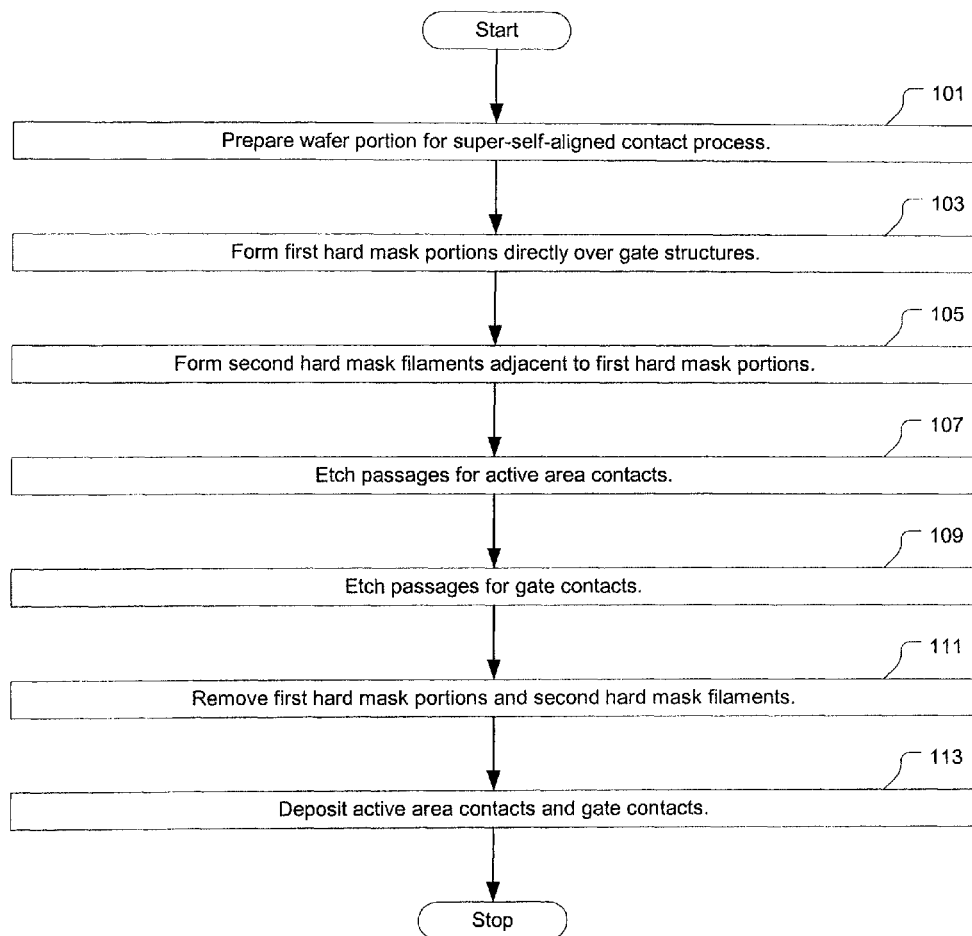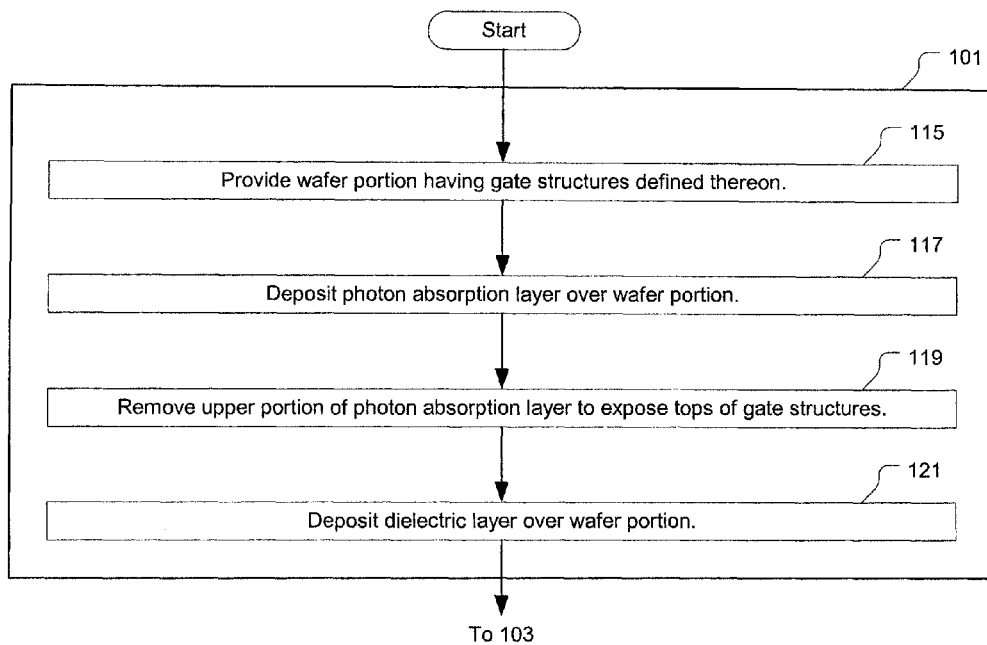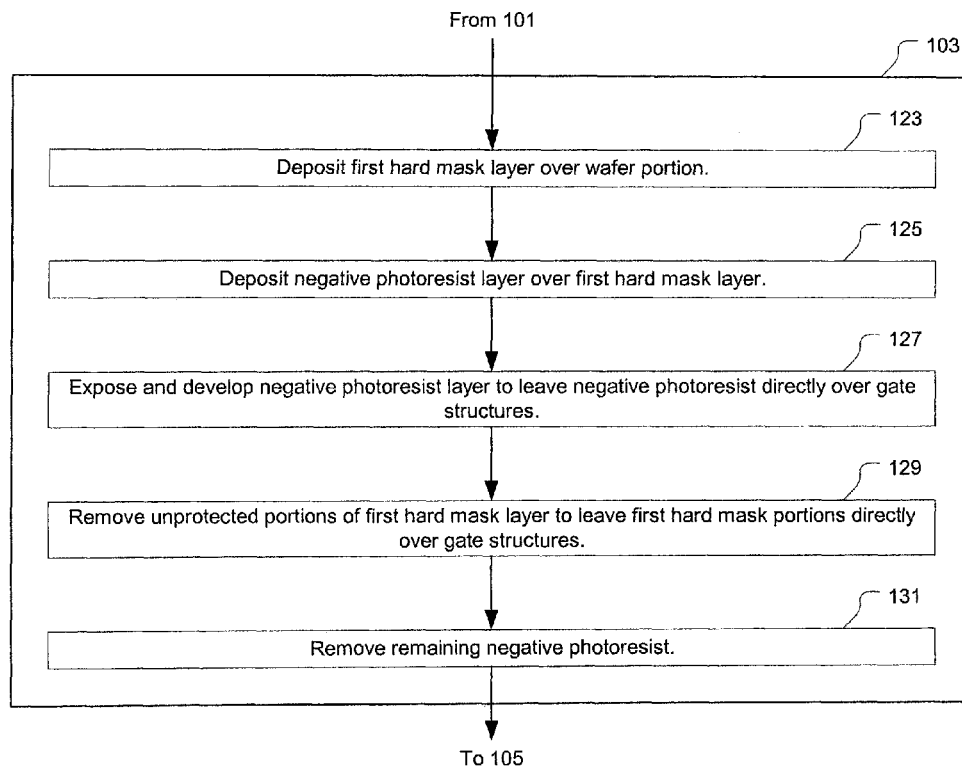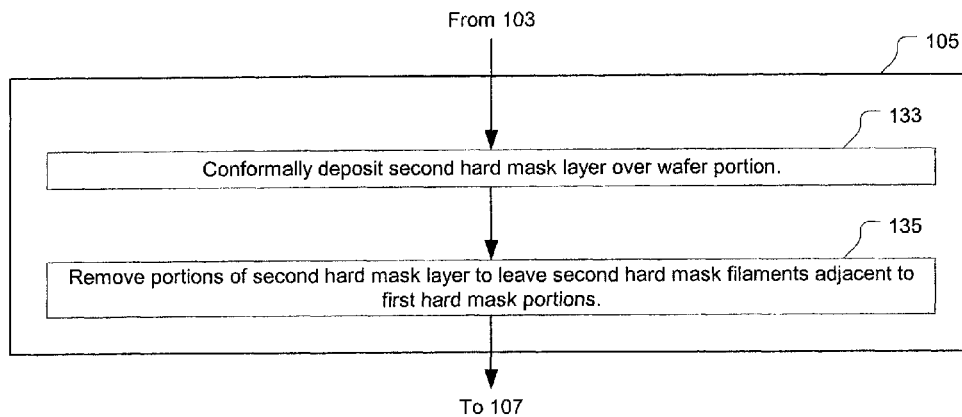
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Start

101
Prepare wafer portion for super-self-aligned contact process.

103
Form first hard mask portions directly over gate structures.

105
Form second hard mask filaments adjacent to first hard mask portions.

107
Etch passages for active area contacts.

109
Etch passages for gate contacts.

111
Remove first hard mask portions and second hard mask filaments.

113
Deposit active area contacts and gate contacts.

Stop

Fig. 1A

Start

101

Provide wafer portion having gate structures defined thereon.

115

Deposit photon absorption layer over wafer portion.

117

Remove upper portion of photon absorption layer to expose tops of gate structures.

119

Deposit dielectric layer over wafer portion.

121

To 103

Fig. 1B

From 101

103

123
Deposit first hard mask layer over wafer portion.

125
Deposit negative photoresist layer over first hard mask layer.

127
Expose and develop negative photoresist layer to leave negative photoresist directly over gate structures.

129
Remove unprotected portions of first hard mask layer to leave first hard mask portions directly over gate structures.

131
Remove remaining negative photoresist.

To 105

Fig. 1C

From 103

105

133
Conformally deposit second hard mask layer over wafer portion.

135
Remove portions of second hard mask layer to leave second hard mask filaments adjacent to first hard mask portions.

To 107

Fig. 1D

From 105

107

137

Deposit positive photoresist layer over wafer portion.

139

Pattern positive photoresist with active area contact mask.

141

Etch passages for active area contacts.

143

Remove patterned positive photoresist.

To 109

Fig. 1E

From 107

109

145

Deposit positive photoresist layer over wafer portion.

147

Pattern positive photoresist with gate contact mask.

149

Etch passages for gate contacts.

151

Remove patterned positive photoresist.

To 111

Fig. 1F

From 111

113

Deposit metal layer over wafer portion so as to fill contact passages.   153

Remove excess metal.   155

Stop

Fig. 1G

Fig. 2A

STI 209

205

207

205

n+ 203

207

205

n+ 203

207

205

n+ 203

207

205

STI 209

n+ 203

207

205

n+ 203

207

205

n+ 203

207

205

n+ 203

207

205

n+ 203

207

205

STI 209

p well 211

p well 211

Substrate 213

View A-A

Fig. 2B

220

215

222

217

219

216

205

215

220

Fig. 2C

Absorption Layer 301

STI 209

n+　n+　n+　n+

p well 211

STI 209

n+

n+　n+　n+

p well 211

STI 209

Substrate 213

View A-A

Fig. 3

View A-A

Fig. 4

Dielectric Layer 501

301

301 n+

301 n+

301 n+

STI 209

301 n+

301 n+

301 n+

301 n+

STI 209

301

p well 211

p well 211

Substrate 213

STI 209

View A-A

Fig. 5

Negative Photoresist Layer 603

First Hard Mask Layer 601

Dielectric Layer 501

605

607

301

STI 209

301   n+

301   n+

301   n+

STI 209

301   n+

p well 211

301   n+

301   n+

301   n+

p well 211

STI 209

301

Substrate 213

View A-A

Fig. 6

603
601
501

701
703
703
703
703
703
703
703
703

301
217
STI 209
301
n+
217
301
n+
217
301
n+
217
p well 211
301
n+
217
STI 209
Substrate 213
301
n+
217
301
n+
217
301
n+
217
p well 211
301
217
STI 209

View A-A

Fig. 7

View A-A

Fig. 8

View A-A

Fig. 9

View A-A

Fig. 10

View A-A

Fig. 11

View A-A

Fig. 12

View A-A

Fig. 13

Fig. 14A

View A-A

Fig. 14B

View A-A

Fig. 15

View A-A

Fig. 16

501

Positive Photoresist Layer 1701

601A 1101A

601A 1101A

601A 1101A

601A 1101A

601A 1101A

601A 1101A

601A 1101A

601A 1101A

301

301

301

301

301

301

301

301

301

301

n+

n+

n+

n+

n+

n+

n+

STI 209

STI 209

p well 211

p well 211

Substrate 213

View A-A

Fig. 17

Fig. 18A

View A-A

Fig. 18B

View A-A

Fig. 19

View A-A

Fig. 20

View A-A

Fig. 21

View A-A

Fig. 22

View A-A

Fig. 23

Fig. 24A

Gate Pitch = P_{GA} = W_{GA} + (2 * S_{GC}) + W_{CT}
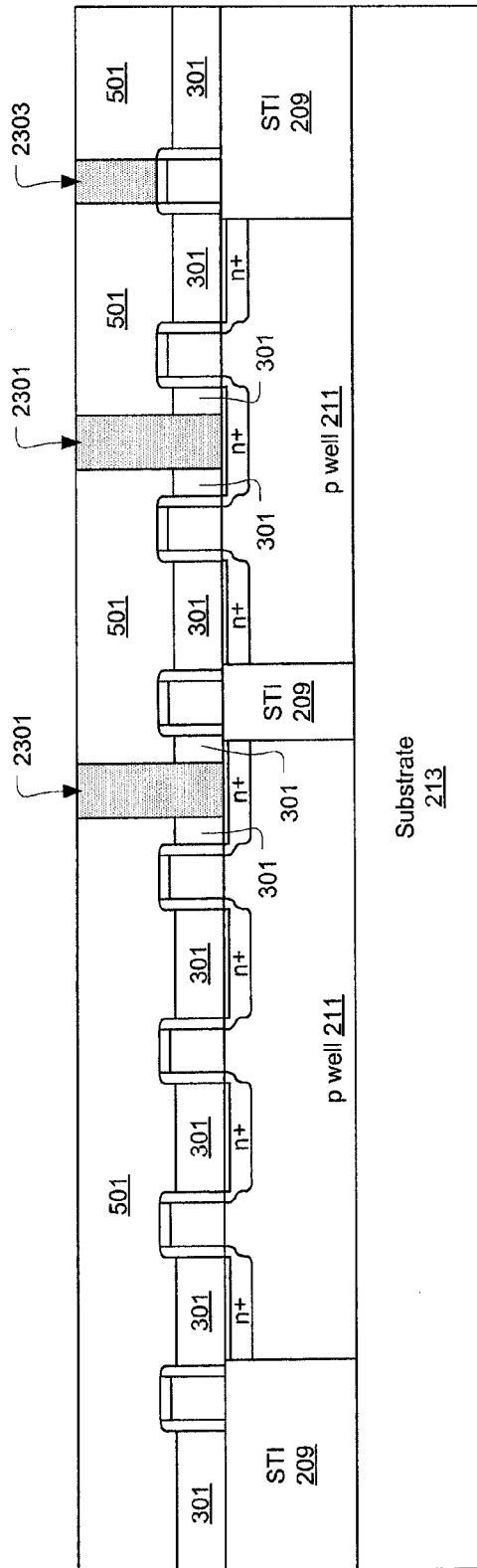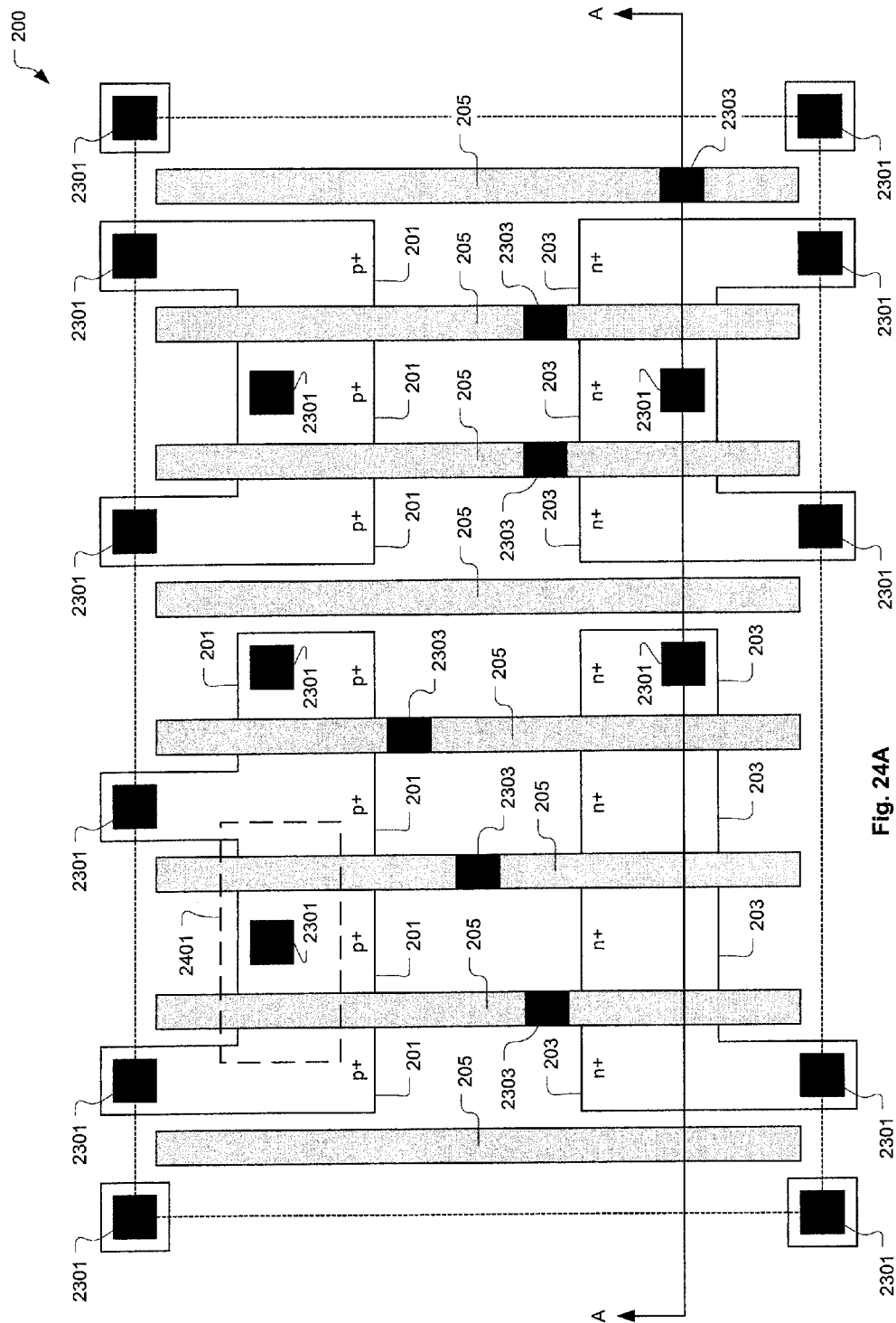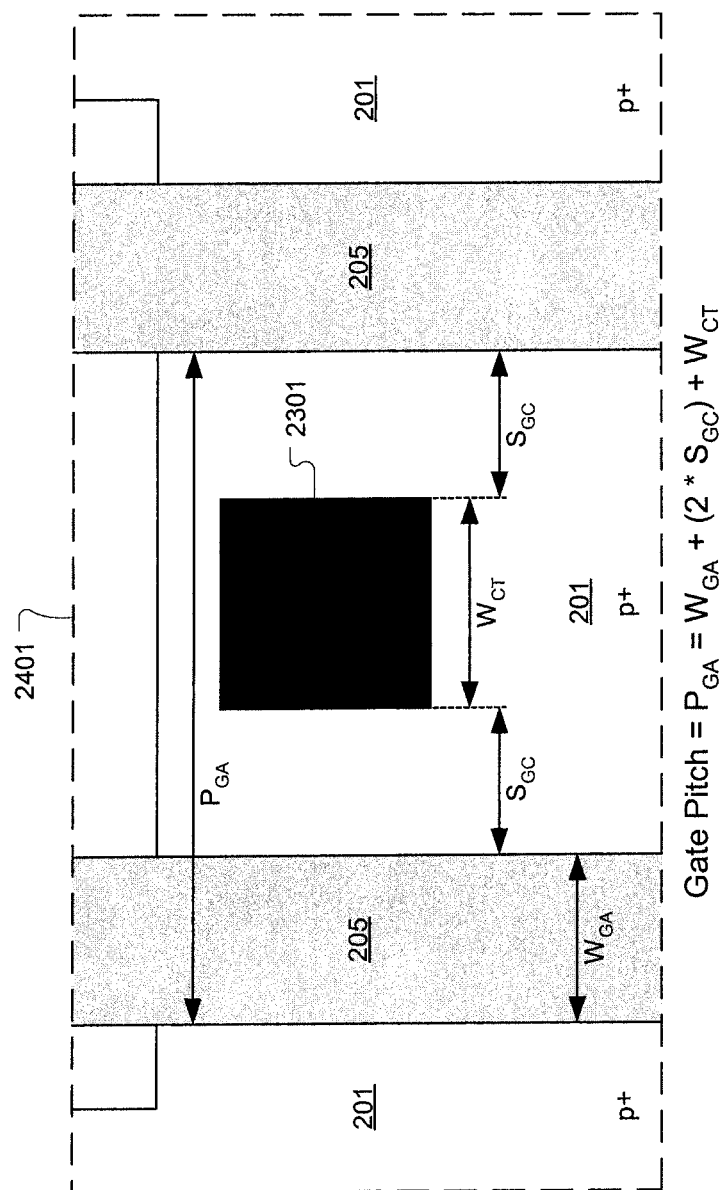
Fig. 24B

SUPER-SELF-ALIGNED CONTACTS AND METHOD FOR MAKING THE SAME

CLAIM OF PRIORITY

This application is a continuation application under 35 U.S.C. 120 of prior U.S. application Ser. No. 14/033,952, filed on Sep. 23, 2013, which is a divisional application under 35 U.S.C. 121 of prior U.S. application Ser. No. 11/956,305, filed Dec. 13, 2007, issued as U.S. Pat. No. 8,541,879, on Sep. 24, 2013. The disclosure of each above-identified patent application is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

During semiconductor wafer fabrication, electrically conductive active area contacts are formed between active areas at the substrate level of the wafer and electrically conductive interconnect lines located above the substrate level. Also, electrically conductive gate contacts are formed between transistor gate structures within the wafer and electrically conductive interconnect lines located above the gate structures. Conventional active area contact and gate contact fabrication methods have relied upon photolithographic techniques in which a photomask is used to project a light pattern onto a photoresist layer deposited on the wafer, so as to transfer the pattern to the photoresist layer, wherein the pattern defines various openings within the photoresist layer at which contacts are to be formed. The various contacts are required to be accurately aligned to the underlying active areas and gate features for proper contact placement, and ultimately for proper device operation. Therefore, the photomask must be accurately aligned to the wafer to enable proper transfer of the contact pattern onto the wafer.

As device sizes become smaller and their features become more closely spaced on the wafer, contact placement and fabrication becomes more difficult. For example, it becomes more difficult to satisfy the increasing photomask-to-wafer alignment accuracy requirements. Therefore, it is of interest to seek methods by which contacts can be more accurately placed and fabricated for devices having smaller and more closely spaced features.

SUMMARY

In one embodiment, a method is disclosed for fabricating an active area contact within a semiconductor wafer. In the method, a number of first hard mask portions are formed over a corresponding number of underlying gate structures, such that each first hard mask portion vertically shadows a respective one of the underlying gate structures. Also in the method, a number of second hard mask filaments are formed adjacent to each of the number of first hard mask portions. A combined width of each first hard mask portion and its adjoining second hard mask filaments is greater than a width of the respective underlying gate structure. Also, a width of each second hard mask filament defines an active area contact-to-gate structure spacing. The method further includes an operation for etching a passage between facing surfaces of neighboring second hard mask filaments, and through a depth of the semiconductor wafer to an active area. Then, an electrically conductive material is deposited within the passage to form the active area contact.

In another embodiment, a method is disclosed for fabricating a gate contact within a semiconductor wafer. In the method, a first hard mask portion is formed over a gate struc-

ture within a section of the semiconductor wafer, such that the first hard mask portion vertically shadows the gate structure. Also, the first hard mask portion is formed to include substantially vertical side surfaces. Also in the method, a second hard mask filament is formed adjacent to each side surface of the first hard mask portion. An etching operation is then performed to etch a passage through the first hard mask portion, and through a depth of the semiconductor wafer to a top surface of the gate structure. During this etching operation, surfaces of the second hard mask filaments adjacent to the vertical side surfaces of the first hard mask portion are revealed through etching of the first mask portion. The revealed side surfaces of the first hard mask portion define side surfaces of the passage. The method then proceeds with an operation for depositing an electrically conductive material within the passage to form the gate contact.

In another embodiment, a method is disclosed for fabricating an active area contact and a gate contact within a semiconductor wafer. The method includes an operation for depositing a photon absorption layer between gate structures within a section of the semiconductor wafer, so as to substantially cover an area present between gate structures with the photon absorption layer while leaving a top surface of each gate structure uncovered. Then, a dielectric layer is deposited over both the photon absorption layer and the top of each gate structure within the section of the semiconductor wafer. The method continues with forming a number of first hard mask portions on the dielectric layer and over the gate structures within the section of the semiconductor wafer. Each first hard mask portion vertically shadows a respective one of the gate structures. Also, each first hard mask portion includes substantially vertical side surfaces. The method then proceeds with forming a second hard mask filament adjacent to each vertical side surface of each first hard mask portion, such that each second hard mask filament has an exposed side surface. A width of each second hard mask filament defines an active area contact-to-gate structure spacing. The method also includes an operation for etching a first passage between facing exposed side surfaces of a given pair of neighboring second hard mask filaments, and through a depth of the semiconductor wafer to an active area. The method further includes an operation for etching a second passage through a given first hard mask portion, and through a depth of the semiconductor wafer to a top surface of the gate structure underlying the given first hard mask portion. Surfaces of the second hard mask filaments adjacent to the vertical side surfaces of the given first hard mask portion are revealed through etching of the given first mask portion. These revealed surfaces of the second hard mask filaments define side surfaces of the second passage. The method then proceeds with an operation for depositing an electrically conductive material within both the first and second passages to respectively form the active area contact and the gate contact.

In another embodiment, a semiconductor device is disclosed. The semiconductor device includes a linear gate structure having side surfaces and a top surface. A width of the linear gate structure is defined by a perpendicular distance between the side surfaces of the linear gate structure. The semiconductor device also includes a gate contact disposed to electrically connect to the top surface of the linear gate structure. The gate contact has a substantially rectangular horizontal cross-section. Also, the gate contact is defined to substantially cover the width of the linear gate structure without extending substantially beyond either of the side surfaces of the gate structure.

Other aspects and advantages of the invention will become more apparent from the following detailed description, taken

in conjunction with the accompanying drawings, illustrating by way of example the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is an illustration showing a flowchart of a method for fabricating super-self-aligned contacts within a semiconductor wafer, in accordance with one embodiment of the present invention;

FIG. 1B is an illustration showing an expanded view of operation 101 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 1C is an illustration showing an expanded view of operation 103 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 1D is an illustration showing an expanded view of operation 105 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 1E is an illustration showing an expanded view of operation 107 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 1F is an illustration showing an expanded view of operation 109 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 1G is an illustration showing an expanded view of operation 113 of FIG. 1A, in accordance with one embodiment of the present invention;

FIG. 2A is an illustration showing a top view of the wafer portion, in accordance with one embodiment of the present invention;

FIG. 2B is an illustration showing a vertical cross-section view of the wafer portion, in accordance with one embodiment of the present invention;

FIG. 2C is an illustration showing the an expanded view of a given gate structure, in accordance with one embodiment of the present invention;

FIG. 3 is an illustration showing the photon absorption layer deposited over the wafer portion, in accordance with one embodiment of the present invention;

FIG. 4 is an illustration showing the upper portion of the photon absorption layer removed to expose the top surfaces of the gate structures, in accordance with one embodiment of the present invention;

FIG. 5 is an illustration showing the dielectric layer deposited over the wafer portion, in accordance with one embodiment of the present invention;

FIG. 6 is an illustration showing the first hard mask layer deposited over the dielectric layer, and the negative photoresist layer deposited over the first hard mask layer, in accordance with one embodiment of the present invention;

FIG. 7 is an illustration showing the exposure of the wafer portion to the vertically collimated, incoherent light, in accordance with one embodiment of the present invention;

FIG. 8 is an illustration showing the wafer portion following removal of the non-cross-linked portions of the negative photoresist layer, in accordance with one embodiment of the present invention;

FIG. 9 is an illustration showing the wafer portion following removal of the unprotected portions of the first hard mask layer, in accordance with one embodiment of the present invention;

FIG. 10 is an illustration showing the wafer portion following removal of the remaining negative photoresist portions, in accordance with one embodiment of the present invention;

FIG. 11 is an illustration showing the second hard mask layer deposited over the wafer portion, in accordance with one embodiment of the present invention;

FIG. 12 is an illustration showing the second hard mask filaments adjacent to the first hard mask portions, in accordance with one embodiment of the present invention;

FIG. 13 is an illustration showing the positive photoresist layer deposited over the wafer portion, in accordance with one embodiment of the present invention;

FIG. 14A is an illustration showing an example active area contact mask used to pattern the positive photoresist layer, in accordance with one embodiment of the present invention;

FIG. 14B is an illustration showing the vertical cross-section view A-A of the wafer portion with the patterned positive photoresist layer, in accordance with one embodiment of the present invention;

FIG. 15 is an illustration showing the vertical cross-section view A-A of the wafer portion with the passages for the active area contacts etched therein, in accordance with one embodiment of the present invention;

FIG. 16 is an illustration showing the wafer portion following removal of the patterned photoresist layer, in accordance with one embodiment of the present invention;

FIG. 17 is an illustration showing the positive photoresist layer deposited over the wafer portion, in accordance with one embodiment of the present invention;

FIG. 18A is an illustration showing an example gate contact mask used to pattern the positive photoresist layer, in accordance with one embodiment of the present invention;

FIG. 18B is an illustration showing the vertical cross-section view A-A of the wafer portion with the patterned positive photoresist layer, in accordance with one embodiment of the present invention;

FIG. 19 is an illustration showing the vertical cross-section view A-A of the wafer portion with the passages for the gate contacts etched therein, in accordance with one embodiment of the present invention;

FIG. 20 is an illustration showing the wafer portion following removal of the patterned photoresist layer, in accordance with one embodiment of the present invention;

FIG. 21 is an illustration showing the wafer portion following removal of the first hard mask portions and the second hard mask filaments, in accordance with one embodiment of the present invention;

FIG. 22 is an illustration showing the vertical cross-section view A-A of the wafer portion with the metal layer deposited thereon, in accordance with one embodiment of the present invention;

FIG. 23 is an illustration showing the vertical cross-section view A-A of the wafer portion with the excess metal layer removed to leave the active area contacts and the gate contacts, in accordance with one embodiment of the present invention;

FIG. 24A is an illustration showing a top view of the wafer portion following formation of the active area contacts and gate contacts, in accordance with one embodiment of the present invention; and

FIG. 24B is an illustration showing an expanded view of an area, as called out in FIG. 24A, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

FIGS. 1A-1G are illustrations showing a flowchart of a method for fabricating super-self-aligned (SSA) contacts within a semiconductor wafer ("wafer" hereafter), in accordance with one embodiment of the present invention. The SSA contacts fabricated according to the method of FIGS. 1A-1G can be either active area contacts or gate contacts. To facilitate description, FIGS. 2A-24B illustrate physical representations of a portion of the wafer as it is subjected to the operations of the method of FIGS. 1A-1G. The method begins with an operation 101 for preparing a wafer portion for the SSA contact process. FIG. 1B is an illustration showing an expanded view of operation 101, in accordance with one embodiment of the present invention. As shown in FIG. 1B, operation 101 includes an operation 115 for providing the wafer portion upon which the SSA contacts are to be fabricated.

FIGS. 2A-2C are illustrations showing an exemplary wafer portion 200 provided in operation 115. It should be understood that the exemplary wafer portion 200 is provided by way of example for the purpose of describing the SSA contact fabrication method of FIGS. 1A-1G. It should be further understood that the SSA contact fabrication method disclosed herein is not to be limited to use with the particular exemplary wafer portion 200. Moreover, it should be appreciated that the SSA contact fabrication process disclosed herein can be performed on essentially any semiconductor device or semiconductor wafer within which one or more active area contacts and/or one or more gate contacts are to be defined.

FIG. 2A is an illustration showing a top view of the wafer portion 200, in accordance with one embodiment of the present invention. FIG. 2B is an illustration showing a vertical cross-section view of the wafer portion 200, in accordance with one embodiment of the present invention. The vertical cross-section view (A-A) of FIG. 2B corresponds to the vertical cross-section of the wafer portion 200 at a location corresponding to bracket A-A in FIG. 2A. The wafer portion 200 includes a number of gate structures 205 defined thereon in a parallel orientation with respect to each other. FIG. 2C is an illustration showing an expanded view of a given gate structure 205, in accordance with one embodiment of the present invention. It should be understood that the given gate structure 205, as shown in FIG. 2C, is representative of the other gate structures 205 within the wafer portion 200.

Each gate structure 205 is defined as a linear gate structure having a central conductive region 219, a top region 217, and sidewall spacers 215. In various embodiments, the central conductive region 219 can be formed of polysilicon, metal, or essentially any other suitable electrically conductive material. The top region 217 is formed of an electrically conductive material that is capable of reflecting photons, such a those of incoherent light. For example, in one embodiment, the top region 217 is formed of $NiSi_2$. In various embodiments, the sidewall spacers 215 can be formed of essentially any suitable material. For example, in one embodiment, the sidewall spacers 215 are formed of Si_3N_4.

Each gate structure 205 is defined as a linear gate structure having a top surface 222, substantially parallel side surfaces 220, a width 216 defined perpendicularly between the side surfaces 220, and a length 218 extending perpendicular to the width 216 along the top surface 222. In the exemplary wafer portion 200, for ease of description, each linear gate structure 205 is shown to have a length approximately equal to the length 218. However, it should be understood that the various gate structures 205 are not required to have the same length. For example, any number of the linear gate structures 205 may be segmented to include a number of breaks, depending on the circuit function to be defined.

Each linear gate structure 205, or segment thereof, is devoid of a substantial change in direction along its length. In one embodiment, a substantial change in direction of a linear gate structure 205, or segment thereof, exists when the width 216 of the linear gate structure 205 at any point thereon changes by more than 50% of the nominal width 216 of the linear gate structure 205 along its entire length. In another embodiment, a substantial change in direction of a linear gate structure 205, or segment thereof, exists when the width 216 of the linear gate structure 205 changes from any first location on the linear gate structure 205 to any second location on the linear gate structure 205 by more than 50% of the width 216 at the first location.

The exemplary wafer portion 200 further includes a number of active areas 203 for NMOS devices, as denoted by (n+), and a number of active areas 201 for PMOS devices, as denoted by (p+). As shown in the cross-section view A-A of FIG. 2B, the n+ active areas 203 are disposed within a "p well" 211, and the p wells 211 are bordered by shallow trench isolation (STI) regions 209. It should be appreciated that in some embodiments the p wells 211 can extend under the STI regions 209. The wafer portion 200, including the p wells 211, the STI regions 209 and the gate structures 205 thereabove, is defined over a substrate 213, such as a silicon substrate. Additionally, the active area regions 201/203 between the sidewalls 215 of each gate structure 205 can be defined to have an exposed conductive surface 207. In one embodiment, the exposed conductive surface 207 is formed of metal, metal silicide, or a combination thereof. For example, in one embodiment, a salicide process is performed to form a nickel silicide as the exposed conductive surface 207 present over portions of the active area regions 201/203.

Additionally, the wafer portion 200 can include a thin, e.g., 200-300 angstroms thick, etch stop and/or stress liner conformally disposed over its top surface, i.e., conformally disposed over the upper exposed surfaces of the substrate 213, STI regions 209, active area regions 201/203, and gate structures 205. For clarity purposes, the etch stop and/or stress liner is not shown in FIGS. 2A-24B. However, it should be understood that such a conformal layer can be present, if appropriate.

Although the wafer portion 200 provided for the SSA contact process has been described in some detail in FIGS. 2A-2C, it should be understood that the SSA contact process is not restricted to the specifically disclosed features of the exemplary wafer portion 200. In other embodiments, the SSA contact process described herein can be used to defined contacts on a semiconductor wafer portion that includes either more or less features than what are explicitly disclosed herein with regard to the exemplary wafer portion 200, so long as the top surface 222 and/or top region 217 of each gate structure is capable of reflecting photons.

With reference back to FIG. 1B, from the operation 115, the method proceeds with an operation 117 for depositing a photon absorption layer 301 over the wafer portion 200. In one embodiment the photon absorption layer 301 is formed of amorphous carbon. However, it should be understood that in other embodiments the photon absorption layer 301 can be formed from essentially any material that has a sufficiently strong photon absorption property and has adequate chemical, structural, thermal, and electrical properties as required for successful manufacture and operation of the semiconductor device formed on the wafer portion 200. In one embodiment, the sufficiently strong photon absorption property of the photon absorption layer 301 material is evidenced by a minimal backscattering of photons incident upon a surface of the photon absorption layer 301 material.

FIG. 3 is an illustration showing the photon absorption layer 301 deposited over the wafer portion 200, in accordance with one embodiment of the present invention. The photon absorption layer 301 is initially deposited to fill the regions between the gate structures 205, and to extend up to a level above the top surfaces 222 of the gate structures 205. An operation 119 is then performed to remove an upper portion of the photon absorption layer 301 so as to expose the top surfaces 222 of the gate structures 205. FIG. 4 is an illustration showing the upper portion of the photon absorption layer 301 removed to expose the top surfaces 222 of the gate structures 205, in accordance with one embodiment of the present invention.

In various embodiments, the removal of the upper portion of the photon absorption layer 301 in operation 119 can be performed using an etching process, a chemical mechanical planarization (CMP) process, or a combination thereof. It should be understood that through operations 117 and 119, the photon absorption layer 301 is deposited between the gate structures 205 so as to substantially cover an area of the wafer portion 200 present between the gate structures 205 with the photon absorption layer 301, while leaving the top surface 222 of each gate structure 205 uncovered. In other words, following operation 119, the photon absorption layer 301 fills regions adjacent to each gate structure 205 so as to contact the side surfaces 220 of each gate structure 205 without covering the top surface 222 of each gate structure 205.

Following operation 119, an operation 121 is performed to deposit a dielectric layer 501, i.e., a pre-metal dielectric layer, over the wafer portion 200. FIG. 5 is an illustration showing the dielectric layer 501 deposited over the wafer portion 200, in accordance with one embodiment of the present invention. The dielectric layer 501 is deposited over both the photon absorption layer 301 and the top surface 222 of each gate structure 205. In one embodiment, the dielectric layer 501 is formed of an electrically insulating oxide material. However, it should be understood that the SSA contact fabrication process is not limited to use with a specific type of dielectric layer 501. The dielectric layer 501 can be formed from essentially any material, or stack of materials, having adequate chemical, structural, thermal, and electrical properties as required for successful manufacture and operation of the semiconductor device formed on the wafer portion 200. Additionally, as part of operation 121, an upper surface 503 of the deposited dielectric layer 501 is substantially planarized. In one embodiment, planarization of the dielectric layer 501 upper surface 503 is performed using a CMP process. However, in other embodiments, essentially any technique can be used to planarize the dielectric layer 501, so long as the technique is compatible with the materials present on the wafer portion 200.

With reference back to FIG. 1A, the method proceeds from the operation 101 to an operation 103 in which first hard mask portions 601A are formed directly over the gate structures 205. The term "first" as used herein with regard to the first hard mask portions 601A, distinguishes a material type used to form the first hard mask portions 601A. As will be discussed later, second hard mask filaments 1101A are also used in the SSA fabrication process. The term "second" as used herein with regard to the second hard mask filaments 1101A, distinguishes a material type used to form the second hard mask filaments 1101A, that is different from the "first" material type used to form the first hard mask portions 601A. In operation 103, the first hard mask portions 601A are formed over a corresponding number of underlying gate structures such that each first hard mask portion 601A vertically shadows a respective one of the underlying gate structures 205.

FIG. 1C is an illustration showing an expanded view of operation 103, in accordance with one embodiment of the present invention. As shown in FIG. 1C, operation 103 includes an operation 123 for depositing a first hard mask layer 601 over the wafer portion 200. More specifically, the first hard mask layer 601 is deposited over the dielectric layer 501. An operation 125 is then performed to deposit a negative photoresist layer 603 over the first hard mask layer 601. FIG. 6 is an illustration showing the first hard mask layer 601 deposited over the dielectric layer 501, and the negative photoresist layer 603 deposited over the first hard mask layer 601, in accordance with one embodiment of the present invention. The first hard mask layer 601 can be defined by essentially any suitable hard mask material. For example, in some embodiments, the first hard mask layer 601 can be defined as an advanced patterning film (APF) or as a SiON hard mask. Also, the first hard mask layer 601 can be deposited on the wafer portion 200 using essentially any hard mask deposition technique. For example, in one embodiment, the first hard mask layer 601 is deposited using a chemical vapor deposition (CVD) process.

A negative photoresist material is characterized in that portions of the negative photoresist material that are sufficiently exposed to a light source will made insoluble, i.e., non-removable, in the presence of a developer solution, and underexposed portions of the negative photoresist material will be remain soluble, i.e., removable, in the presence of the developer solution. The negative photoresist layer 603 can be defined by essentially any type of negative photoresist material, e.g., photosensitive polymer, so long as the light exposure threshold for cross-linking of the negative photoresist material is suitable for use with a given light source, such that more than a forward exposure of the negative photoresist material to the given light source is required for cross-linking of the negative photoresist material. For example, the light exposure threshold of the negative photoresist material is such that a transmission of collimated, incoherent light from the given light source through an upper surface 605 of the negative photoresist layer 603 to a lower surface 607 of the negative photoresist layer 603, i.e., forward exposure, is not sufficient to cross-link the negative photoresist material.

However, the light exposure threshold of the negative photoresist material is such that the forward exposure of the negative photoresist material combined with a reflective exposure of the negative photoresist material, i.e., exposure to light reflected upward from below the lower surface 607 of the negative photoresist layer 603, is sufficient to cross-link the negative photoresist material. Also, the characteristics of the light, e.g., intensity, duration, wavelength, etc., incident upon the negative photoresist layer 603 can be controlled in conjunction with the light exposure threshold of the negative photoresist material such that a specific amount of reflective exposure of the negative photoresist material is required for cross-linking of the negative photoresist material. Additionally, it should be understood that the negative photoresist layer 603 can be deposited on the wafer portion 200 using essentially any photoresist deposition technique, such as spin-on deposition.

From the operation 125, the method proceeds with an operation 127 for exposing and developing the negative photoresist layer 603, so as to only leave negative photoresist portions that vertically overlie gate structures 205. In one embodiment, operation 125 is performed by uniformly exposing the negative photoresist layer 603 to vertically collimated, incoherent light, whereby the light passes through the negative photoresist layer 603 to be absorbed by the photon absorption layer 301, and to be reflected by the top

surface 222/top region 217 of the gate structures 205. FIG. 7 is an illustration showing the exposure of the wafer portion 200 to the vertically collimated, incoherent light, in accordance with one embodiment of the present invention. The uniform exposure of the negative photoresist layer 603 to the vertically collimated, incoherent light is depicted by the downward pointing arrows within bracket 701. Reflection of the light, i.e., upward reflection, is depicted by the upward pointing arrows within brackets 703. It should be appreciated that use of incoherent light serves to prevent formation of standing light waves.

Because both forward and reflected exposures of the negative photoresist layer 603 are required to cross-link the negative photoresist, only those portions of negative photoresist that vertically overlie the reflective top surfaces 222/top regions 217 of the gate structures will be cross-linked. Also, it should be appreciated that because the light is vertically collimated to be normally, i.e., perpendicularly, incident upon the top surfaces 222 of the gate structures 205, which are substantially horizontal, only those portions of the negative photoresist layer 603 that are located vertically over the gate structures 205 will be subjected to substantial reflective exposure of the light.

Following exposure of the negative photoresist layer 603 to the light, the negative photoresist layer 603 is developed to remove the non-cross-linked portions of the negative photoresist layer 603. In various embodiments, essentially any photoresist development technique suitable for use with the particular negative photoresist material can be utilized. For example, in one embodiment, an acid etch can be used to remove the non-cross-linked portions of the negative photoresist layer 603. FIG. 8 is an illustration showing the wafer portion 200 following removal of the non-cross-linked portions of the negative photoresist layer 603, in accordance with one embodiment of the present invention. As shown in FIG. 8, exposure and development of the negative photoresist layer 603 in operation 127 leaves the negative photoresist portions 603A, such that each negative photoresist portion 603A vertically overlies a respective one of the underlying gate structures 205.

Following operation 127, the method proceeds with an operation 129 for removing portions of the first hard mask layer 601 that are not protected by the negative photoresist portions 603A, thereby forming the first hard mask portions 601A directly over the gate structures 205. In one embodiment, operation 129 is performed using a vertically biased etching process, such that the portions of the first hard mask layer 601 that are not protected by the negative photoresist portions 603A are removed in a substantially top-down manner. However, it should be understood that other techniques can be used to remove the portions of the first hard mask layer 601 that are not protected by the negative photoresist portions 603A, so long as a width 901 of the remaining first hard mask portions 601A substantially matches a width 903 of the negative photoresist portions 603A. In other words, undercutting of the first hard mask portions 601A relative to the negative photoresist portions 603A should be minimized to the extent possible.

FIG. 9 is an illustration showing the wafer portion 200 following removal of the unprotected portions of the first hard mask layer 601, in accordance with one embodiment of the present invention. As shown in FIG. 9, removal of the unprotected portions of the first hard mask layer 601 in operation 129 leaves the first hard mask portions 601A, such that each first hard mask portion 601A vertically shadows a respective one of the underlying gate structures 205. It should be understood that vertical shadowing of a given underlying gate

structure 205 by a given first hard mask portion 601A is defined by the given first hard mask portion 601A having the substantially same horizontal cross-section size and shape as the given underlying gate structure 205. The horizontal cross-section size and shape refers to the size and shape of the feature, i.e., gate structure 205 or first hard mask portion 601A, when cut in a horizontal plane substantially parallel to the horizontal surface of the substrate 213. It should be further appreciated that the horizontal width 901 of each first hard mask portion 601A is substantially the same as the horizontal width of the top surface 222/top region 217 of the underlying gate structure 205.

Following the operation 129, the method proceed with an operation 131 for removing the remaining negative photoresist portions 603A. Removal of the remaining negative photoresist portions 603A can be performed using essentially any photoresist stripping technique, e.g., chemical stripping, ashing, etc. FIG. 10 is an illustration showing the wafer portion 200 following removal of the remaining negative photoresist portions 603A, in accordance with one embodiment of the present invention.

With reference back to FIG. 1A, the method proceeds from the operation 103 to an operation 105 in which the second hard mask filaments 1101A are formed adjacent to the first hard mask portions 601A. FIG. 1D is an illustration showing an expanded view of operation 105, in accordance with one embodiment of the present invention. As shown in FIG. 1D, operation 105 includes an operation 133 for conformally depositing a second hard mask layer 1101 over the wafer portion 200. FIG. 11 is an illustration showing the second hard mask layer 1101 conformally deposited over the wafer portion 200, in accordance with one embodiment of the present invention. As shown in FIG. 11, the second hard mask layer 1101 is conformally deposited over both the dielectric layer 501 and the first hard mask portions 601A.

The second hard mask layer 1101 can be defined by essentially any suitable hard mask material, so long as the second hard mask material is different from the first hard mask material used to form the first hard mask portions 601A. More specifically, the second hard mask material should have an etching selectivity different than that of the first hard mask material, such that the first hard mask material can be etched without substantially etching the second hard mask material. For example, in one embodiment, the second hard mask layer 1101 can be formed of a nitride material. Also, the second hard mask layer 1101 can be deposited on the wafer portion 200 using essentially any hard mask deposition technique. For example, in one embodiment, the second hard mask layer 1101 is conformally deposited using a chemical vapor deposition (CVD) process.

Following the operation 133, an operation 135 is performed to remove portions of the second hard mask layer 1101 to leave second hard mask filaments 1101A adjacent to the first hard mask portions 601A. FIG. 12 is an illustration showing the second hard mask filaments 1101A adjacent to the first hard mask portions 601A, in accordance with one embodiment of the present invention. The second hard mask filaments 1101A are essentially defined as sidewall spacers adjacent to the first hard mask portions 601A, such that each side surface of each first hard mask portion 601A has an adjoining second hard mask filament 1101A. In one embodiment, a horizontal width 1201 of each second hard mask filament 1101A, as measured perpendicular to the sidewall of its adjoining first hard mask portion 601A, is defined to be substantially the same. Also, in one embodiment, a vertical cross-section profile of each exposed sidewall 1203 of each second hard mask filament 1101A is defined to be substan-

tially vertical. However, in other embodiments, the vertical cross-section profile of the exposed sidewalls 1203 of the hard mask filaments 1101A may other than substantially vertical. For example, in one embodiment, the vertical cross-section profile of the exposed sidewall 1203 of the second hard mask filament 1101A can be tapered such that the second hard mask filament 1101A is thicker at its bottom, i.e., at the dielectric layer 501, relative to its top.

In one embodiment, the second hard mask filaments 1101A are formed by etching the second hard mask layer 1101, such that horizontal surfaces of the second hard mask layer 1101 are preferentially etched relative to the vertical surfaces of the second hard mask layer 1101. It should be understood, however, that other techniques can be utilized to form the second hard mask filaments 1101A from the second hard mask layer 1101, such that each second hard mask filament 1101A is formed as a hard mask spacer extending out from the sidewalls of the first hard mask portions 601A. Because the width 901 of a given first hard mask portion 601A is substantially equal to the width of the top surface 222 of the underlying gate structure 205, a combined width of the given first hard mask portion 601A and its adjoining second hard mask filaments 1101A is greater than the width of the underlying gate structure 205. Also, it should be understood that a perpendicular spacing 1205 between facing exposed side surfaces of a given pair of neighboring second hard mask filaments 1101A effectively defines a width of an active area contact to be formed between the given pair of neighboring second hard mask filaments 1101A. Therefore, because the first hard mask portion 601A vertically shadows the underlying gate structure 205, the width 1201 of each second hard mask filament effectively defines an active area contact-to-gate structure 205 spacing.

With reference back to FIG. 1A, the method proceeds from the operation 105 to an operation 107 in which passages are etched for active area contacts. FIG. 1E is an illustration showing an expanded view of operation 107, in accordance with one embodiment of the present invention. As shown in FIG. 1E, operation 107 includes an operation 137 for depositing a positive photoresist layer 1301 over the wafer portion 200. FIG. 13 is an illustration showing the positive photoresist layer 1301 deposited over the wafer portion 200, in accordance with one embodiment of the present invention. As shown in FIG. 13, the positive photoresist layer 1301 is deposited over both the exposed dielectric layer 501 portions, the exposed first hard mask portions 601A, and the exposed second hard mask filaments 1101A. The positive photoresist layer 1301 can be defined by essentially any type of positive photoresist material. The positive photoresist material is characterized in that portions of the positive photoresist material that are sufficiently exposed to a light source will made soluble, i.e., removable, in the presence of a developer solution, and underexposed portions of the positive photoresist material will remain insoluble, i.e., non-removable, in the presence of the developer solution.

Following operation 137, an operation 139 is performed to pattern the positive photoresist layer 1301 with an active area contact mask. More specifically, the positive photoresist layer 1301 is patterned to include a substantially linear opening through the positive photoresist layer 1301, extending from one first hard mask portion 601A to a neighboring first hard mask portion 601A in a direction substantially perpendicular to the length of each of the neighboring first hard mask portions 601A. The patterning of the positive photoresist layer 1301 can be performed using essentially any conventional photolithography technique.

FIG. 14A is an illustration showing an example active area contact mask used to pattern the positive photoresist layer 1301, in accordance with one embodiment of the present invention. The active area contact mask includes a number of linear openings 1401. Each linear opening 1401 represents an area where the positive photoresist layer 1301 is removed to expose the underlying dielectric layer 501, first hard mask portions 601A, and second hard mask filaments 1101A. Although, the linear openings 1401 are shown as "ideal" rectangular-shaped openings, it should be understood that the actual linear openings 1401 may have somewhat rounded ends. However, it should be noted that the rounded ends will lie above the first hard mask portions 601A and/or the second hard mask filaments 1101A, but not above the dielectric layer 501 portion that extends perpendicularly between the second hard mask filaments 1101A.

FIG. 14B is an illustration showing the vertical cross-section view A-A of the wafer portion 200 with the patterned positive photoresist layer 1301, in accordance with one embodiment of the present invention. Substantially rectangular areas 1403 of the dielectric layer 501 are exposed between the neighboring second hard mask filaments 1101A within the linear openings 1401. The substantially rectangular areas 1403 of the dielectric layer 501 are bounded on two opposing side by the second hard mask filaments 1101A, and on the other two opposing sides by the linear opening 1401 of the patterned positive photoresist layer 1301. It should be appreciated that the substantially rectangular areas 1403 of the dielectric layer 501 represent the horizontal cross-section of the active area contact to be formed.

Also, it should be appreciated that because the active area contact is to be bounded by the second hard mask filaments 1101A in the linear openings 1401, and because the linear openings 1401 are "oversized" with respect to the distance between the sidewalls of the neighboring second hard mask filaments 1101A, there is some flexibility provided in the indexing of the active area contact mask to the wafer portion 200 when patterning the positive photoresist layer 1301. For example, if the linear opening 1401 is offset slightly in its direction of extent between the first hard mask portions 601A, the substantially rectangular area 1403 of exposed dielectric layer 501 will be unaffected.

Following the operation 139, the method proceeds with an operation 141 for etching passages 1501 for the active area contacts. FIG. 15 is an illustration showing the vertical cross-section view A-A of the wafer portion 200 with the passages 1501 etched therein, in accordance with one embodiment of the present invention. The passages 1501 for the active area contacts are etched downward through the exposed, substantially rectangular areas 1403 of the dielectric layer 501 within the linear openings 1401. In one embodiment, the passages 1501 for the active area contacts are etched in a substantially vertical manner, such that sidewalls of the passages 1501 extend in a substantially vertical manner downward from the periphery of the substantially rectangular areas 1403 of the dielectric layer 501 within the linear openings 1401. Although, the sidewalls of the passages 1501 ideally extend downward in a substantially vertical manner, it should be understood that the sidewalls of the passages 1501 can be slightly tapered. For example, in one embodiment, the sidewalls of a given passage 1501 can be tapered such that the rectangular opening of the given passage 1501 is slightly smaller at its bottom end relative to its top end.

In one embodiment, a vertically biased etching process can be used to form the passages 1501 for the active area contacts. The passages 1501 are etched downward through the underlying portion of the dielectric layer 501, and the underlying

portion of the photon absorption layer **301** to reach the conductive material, e.g., silicide, present at the top of the underlying active area, or to reach an etch stop layer present over the underlying active area. It should be understood that during the etching of the passages **1501** for the active area contacts, the second hard mask filaments **1101A** are etched very slowly so as to not be substantially removed.

Following the operation **141**, an operation **143** is performed to remove the patterned photoresist layer **1301** from the wafer portion **200**. FIG. **16** is an illustration showing the wafer portion **200** following removal of the patterned photoresist layer **1301**, in accordance with one embodiment of the present invention. The patterned photoresist layer **1301** can be removed using essentially any photoresist stripping technique, e.g., chemical stripping, ashing, etc.

With reference back to FIG. **1A**, the method proceeds from the operation **107** to an operation **109** in which passages are etched for gate contacts. FIG. **1F** is an illustration showing an expanded view of operation **109**, in accordance with one embodiment of the present invention. As shown in FIG. **1F**, operation **109** includes an operation **145** for depositing a positive photoresist layer **1701** over the wafer portion **200**. FIG. **17** is an illustration showing the positive photoresist layer **1701** deposited over the wafer portion **200**, in accordance with one embodiment of the present invention. As shown in FIG. **17**, the positive photoresist layer **1701** is deposited over both the exposed dielectric layer **501** portions, the exposed first hard mask portions **601A**, the exposed second hard mask filaments **1101A**, and within the active area contact passages **1501** previously etched in operation **107**. The positive photoresist layer **1701** can be defined by essentially any type of positive photoresist material. The positive photoresist material is characterized in that portions of the positive photoresist material that are sufficiently exposed to a light source will made soluble, i.e., removable, in the presence of a developer solution, and underexposed portions of the positive photoresist material will remain insoluble, i.e., non-removable, in the presence of the developer solution.

Following operation **145**, an operation **147** is performed to pattern the positive photoresist layer **1701** with a gate contact mask. More specifically, the positive photoresist layer **1701** is patterned to include a number of substantially linear openings through the positive photoresist layer **1701**, each extending across a given first hard mask portion **601A** and across portions of the two second hard mask filaments **1101A** adjacent to the given first hard mask portion **601A**. The substantially linear opening defined through the positive photoresist layer **1701** is oriented to extend in a direction substantially perpendicular to the length **218** of the underlying gate structure **205** over which the linear opening is defined. The patterning of the positive photoresist layer **1701** can be performed using essentially any conventional photolithography technique.

FIG. **18A** is an illustration showing an example gate contact mask used to pattern the positive photoresist layer **1701**, in accordance with one embodiment of the present invention. The gate contact mask includes a number of linear openings **1801**. Each linear openings **1801** represents area where the positive photoresist layer **1701** is removed to expose the underlying first hard mask portion **601A**, and adjoining portions of the second hard mask filaments **1101A**. Although, the linear openings **1801** are shown as "ideal" rectangular-shaped openings, it should be understood that the actual linear openings **1801** may have somewhat rounded ends. However, it should be noted that the rounded ends of a given linear opening **1801** will lie above the adjoining second hard mask fila-

ments **1101A**, and will not lie above the first hard mask portion **601A** over which the given linear opening **1801** extends.

FIG. **18B** is an illustration showing the vertical cross-section view A-A of the wafer portion **200** with the patterned positive photoresist layer **1701**, in accordance with one embodiment of the present invention. Substantially rectangular areas **1803** of first hard mask portions **601A** are exposed between the neighboring second hard mask filaments **1101A** within the linear openings **1801**. The substantially rectangular areas **1803** of the first hard mask portions **601A** are bounded on two opposing side by the second hard mask filaments **1101A**, and on the other two opposing sides by the linear opening **1801** of the patterned positive photoresist layer **1701**. It should be appreciated that the substantially rectangular area **1803** of the first hard portion **601A**, as exposed in the linear opening **1801**, represents the horizontal cross-section of the gate contact to be formed. Also, it should be appreciated that because the gate contact is to be bounded by the second hard mask filaments **1101A** in the linear opening **1801**, and because the linear opening **1801** is "oversized" with respect to the width of the first hard mask portion **601A**, there is some flexibility provided in the indexing of the gate contact mask to the wafer portion **200** when patterning the positive photoresist layer **1701**. For example, if the linear opening **1801** is offset slightly in its direction of extent between the second hard mask filaments **1101A**, the substantially rectangular area **1803** of the exposed first hard mask portion **601A** will be unaffected.

Following the operation **147**, the method proceeds with an operation **149** for etching passages **1901** for the gate contacts. FIG. **19** is an illustration showing the vertical cross-section view A-A of the wafer portion **200** with the passages **1901** etched therein, in accordance with one embodiment of the present invention. The passages **1901** for the gate contacts are etched downward through the exposed, substantially rectangular areas **1803** of the first hard mask portion **601A** within the linear openings **1801**. It should be appreciated that because the materials of the first hard mask portion **601A** and the second hard mask filament **1101A** are different, these material can be selected to have a substantially different etching selectivity with respect to a given etching process. For example, the first hard mask portion **601A** may be defined to etch ten times faster than the second hard mask filaments **1101A**. Therefore, during the particular etching process to be performed in operation **149**, the exposed first hard mask portion **601A** is defined to be preferentially etched without substantially affecting the neighboring exposed second hard mask filaments **1101A**. It should be understood that during the etching of the passages **1901** for the gate contacts, the second hard mask filaments **1101A** are etched very slowly so as to not be substantially removed.

In one embodiment, the passages **1901** for the gate contacts are etched in a substantially vertical manner, such that sidewalls of the passages **1901** extend in a substantially vertical manner downward from the periphery of the substantially rectangular areas **1803** of the exposed first hard mask portion **601A** within the linear openings **1801**. However, it should be understood that the sidewalls of the passages **1901** are not required to extend downward in a substantially vertical manner. For example, in one embodiment, the sidewalls of the passages **1901** can be slightly tapered, such that the rectangular opening of the given passage **1901** is slightly smaller at its bottom end relative to its top end. In one embodiment, a vertically biased etching process can be used to form the passages **1901** for the gate contacts. The passages **1901** are etched downward through the first hard mask portion **601A** to

reach the top surface 222 of the underlying gate structure 205, or to reach an etch stop layer present over the underlying gate structure 205.

Following the operation 149, an operation 151 is performed to remove the patterned photoresist layer 1701 from the wafer portion 200. FIG. 20 is an illustration showing the wafer portion 200 following removal of the patterned photoresist layer 1701, in accordance with one embodiment of the present invention. The patterned photoresist layer 1701 can be removed using essentially any photoresist stripping technique, e.g., chemical stripping, ashing, etc.

With reference back to FIG. 1A, the method proceeds from the operation 109 to an operation 111 in which the first hard mask portions 601A and the second hard mask filaments 1101A are removed from the wafer portion 200. FIG. 21 is an illustration showing the wafer portion 200 following removal of the first hard mask portions 601A and the second hard mask filaments 1101A, in accordance with one embodiment of the present invention. Operation 111 can be performed using essentially any hard mask removal technique. For example, in one embodiment the first hard mask portions 601A and the second hard mask filaments 1101A are removed using a wet stripping technique. It should also be understood that the operation 111 includes removal of any exposed etch stop layer, if present at the bottoms of the passages 1501 and 1901.

The method proceeds from operation 111 to an operation 113 in which active area contacts 2301 and gate contacts 2303 are disposed within the passages 1501 and 1901, respectively. FIG. 1G is an illustration showing an expanded view of operation 113, in accordance with one embodiment of the present invention. As shown in FIG. 1G, operation 113 includes an operation 153 for depositing a metal layer 2201 over the wafer portion 200. FIG. 22 is an illustration showing the vertical cross-section view A-A of the wafer portion 200 with the metal layer 2201 deposited thereon, in accordance with one embodiment of the present invention. In one embodiment, the metal layer 2201 is deposited as a liner followed by a metal fill. For example, in one embodiment, the metal layer 2201 is formed by first depositing a TiN liner over the wafer portion 200 using a chemical vapor deposition (CVD) process or a physical vapor deposition (PVD) process. Then, a tungsten (W) fill layer is deposited over the TiN liner using a CVD process. In this embodiment, the TiN liner is relatively thin, while the W fill layer completely fills the contact passages 1501 and 1901.

Following the operation 153, an operation 155 is performed to removal excess metal from the top of the wafer portion 200, so as to leave the top surface of the dielectric layer exposed 501 and the contact passages 1501 and 1901 filled with metal. For example, in the TiN liner/W fill embodiment, a CMP process can be used to perform operation 155 so as to remove the W fill layer and the TiN liner from the top surface of the dielectric layer 501. FIG. 23 is an illustration showing the vertical cross-section view A-A of the wafer portion 200 with the excess metal layer 2201 removed to leave the active area contacts 2301 and the gate contacts 2303, in accordance with one embodiment of the present invention. Following completion of operation 113, i.e., following completion of the SSA contact fabrication process, fabrication of the wafer portion 200 can continue with fabrication of a metalization layer over the dielectric layer 501.

FIG. 24A is an illustration showing a top view of the wafer portion 200 following formation of the active area contacts 2301 and gate contacts 2303, in accordance with one embodiment of the present invention. It should be appreciated that each active area contact 2301 is substantially centered between its neighboring gate structures 205. Also, it should

be appreciated that each gate contact 2303 is defined to substantially cover the width of the underlying gate structure 205 without extending substantially beyond either of the side surfaces of the underlying gate structure 205. Hence, due to their direct reference from the as-fabricated gate structures 205, the active area contacts 2301 and the gate contacts 2303 are considered to be super-self-aligned (SSA) contacts with respect to the gate structures 205. Additionally, it should be appreciated that the horizontal cross-section of each active area contact and each gate contact is substantially rectangular in shape.

FIG. 24B is an illustration showing an expanded view of an area 2401, as called out in FIG. 24A, in accordance with one embodiment of the present invention. As shown in FIG. 24B, the active area contact 2301 is substantially centered between its neighboring gate structures 205, such that a substantially equal gate-to-active area contact spacing (SGC) exists on each side the active area contact 2301. As previously discussed, the gate-to-active area contact spacing (SGC) is defined by the width of the second hard mask filament 1101A, as measured in the horizontal direction perpendicular to the length 218 of the gate structure 205. As shown in FIG. 24B, the gate pitch (PGA) is equal to the sum of the gate width (WGA), the active area contact width (WCT), and twice the gate-to-active area contact spacing (SGC).

While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:

a first linear gate structure having side surfaces oriented in a first direction and a top surface, wherein a width of the first linear gate structure is defined by a distance extending in a second direction perpendicular to the first direction between the side surfaces of the first linear gate structure, the first linear gate structure forming a gate electrode of at least one transistor;

a second linear gate structure having side surfaces oriented in the first direction and a top surface, wherein a width of the second linear gate structure is defined by a distance extending in the second direction between the side surfaces of the second linear gate structure, the second linear gate structure forming a gate electrode of at least one transistor;

a first gate contact in physical contact with the top surface of the first linear gate structure, the first gate contact formed to cover the width of the first linear gate structure without extending in the second direction substantially beyond either of the side surfaces of the first linear gate structure; and

a second gate contact in physical contact with the top surface of the second linear gate structure, the second gate contact formed to cover the width of the second linear gate structure without extending in the second direction substantially beyond either of the side surfaces of the second linear gate structure,

wherein the first and second gate contacts are positioned in a side-by-side configuration, such that a virtual line oriented in the second direction extends through both the first and second gate contacts.

2. The semiconductor device as recited in claim 1, wherein the first gate contact extends in the first direction from a first

end to a second end, and wherein the second gate contact extends in the first direction from a first end to a second end, and wherein the first end of the first gate contact and the first end of the second gate contact are substantially aligned with a first virtual line oriented in the second direction.

3. The semiconductor device as recited in claim 2, wherein the second end of the first gate contact and the second end of the second gate contact are substantially aligned with a second virtual line oriented in the second direction

4. The semiconductor device as recited in claim 1, wherein the top surface of the first linear gate structure is formed of a photon reflecting material, and wherein the top surface of the second linear gate structure is formed of the photon reflecting material.

5. The semiconductor device as recited in claim 4, further comprising:
sidewall spacers respectively disposed along the side walls of the first linear gate structure and the second linear gate structure.

6. The semiconductor device as recited in claim 5, further comprising:
a photon absorption material disposed adjacent to the sidewall spacers.

7. The semiconductor device as recited in claim 6, further comprising:
a dielectric material disposed over the photon absorption material, the sidewall spacers, the first linear gate structure, and the second linear gate structure, wherein the dielectric material includes an opening in which the first gate contact is disposed and an opening in which the second gate contact is disposed.

8. The semiconductor device as recited in claim 1, wherein the first linear gate structure forms a gate electrode of a transistor of a first transistor type, and wherein the second linear gate structure forms a gate electrode of a transistor of the first transistor type.

9. The semiconductor device as recited in claim 1, wherein the first linear gate structure forms a gate electrode of a transistor of a first transistor type, and wherein the second linear gate structure forms a gate electrode of a transistor of a second transistor type.

10. The semiconductor device as recited in claim 1, further comprising:
a third linear gate structure having side surfaces oriented in the first direction and a top surface, wherein a width of the third linear gate structure is defined by a distance extending in the second direction between the side surfaces of the third linear gate structure, the width of the third linear gate structure substantially equal to the width of each of the first and second linear gate structures,
wherein the first, second, and third linear gate structures are positioned in accordance with a substantially equal centerline-to-centerline pitch as measured in the second direction, and
wherein the third linear gate structure does not form a gate electrode of any transistor.

11. A semiconductor device, comprising:
a first linear gate structure having side surfaces oriented in a first direction and a top surface, wherein a width of the first linear gate structure is defined by a distance extending in a second direction perpendicular to the first direction between the side surfaces of the first linear gate structure, the first linear gate structure forming a gate electrode of at least one transistor;
a second linear gate structure having side surfaces oriented in the first direction and a top surface, wherein a width of

the second linear gate structure is defined by a distance extending in the second direction between the side surfaces of the second linear gate structure, the second linear gate structure forming a gate electrode of at least one transistor;
a first gate contact in physical contact with the top surface of the first linear gate structure, the first gate contact formed to cover the width of the first linear gate structure without extending in the second direction substantially beyond either of the side surfaces of the first linear gate structure; and
a second gate contact in physical contact with the top surface of the second linear gate structure, the second gate contact formed to cover the width of the second linear gate structure without extending in the second direction substantially beyond either of the side surfaces of the second linear gate structure,
wherein the first and second linear gate structures are positioned in a side-by-side configuration, such that no other linear gate structure is positioned between the first and second linear gate structures,
wherein the first and second gate contacts are positioned in an offset configuration, such that no virtual line oriented in the second direction extends through both the first and second gate contacts.

12. The semiconductor device as recited in claim 11, wherein the first gate contact has a length as measured in the first direction, and wherein the second gate contact has a length as measured in the first direction, and wherein the length of the first gate contact is substantially equal to the length of the second gate contact.

13. The semiconductor device as recited in claim 11, wherein the top surface of the first linear gate structure is formed of a photon reflecting material, and wherein the top surface of the second linear gate structure is formed of the photon reflecting material.

14. The semiconductor device as recited in claim 13, further comprising:
sidewall spacers respectively disposed along the side walls of the first linear gate structure and the second linear gate structure.

15. The semiconductor device as recited in claim 14, further comprising:
a photon absorption material disposed adjacent to the sidewall spacers.

16. The semiconductor device as recited in claim 15, further comprising:
a dielectric material disposed over the photon absorption material, the sidewall spacers, the first linear gate structure, and the second linear gate structure, wherein the dielectric material includes an opening in which the first gate contact is disposed and an opening in which the second gate contact is disposed.

17. The semiconductor device as recited in claim 11, wherein the first linear gate structure forms a gate electrode of a transistor of a first transistor type, and wherein the second linear gate structure forms a gate electrode of a transistor of the first transistor type.

18. The semiconductor device as recited in claim 11, wherein the first linear gate structure forms a gate electrode of a transistor of a first transistor type, and wherein the second linear gate structure forms a gate electrode of a transistor of a second transistor type.

19. The semiconductor device as recited in claim 11, further comprising:
a third linear gate structure having side surfaces oriented in the first direction and a top surface, wherein a width of

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the third linear gate structure is defined by a distance extending in the second direction between the side surfaces of the third linear gate structure, the width of the third linear gate structure substantially equal to the width of each of the first and second linear gate structures,

wherein the first, second, and third linear gate structures are positioned in accordance with a substantially equal centerline-to-centerline pitch as measured in the second direction, and

wherein the third linear gate structure does not form a gate electrode of any transistor.

20. The semiconductor device as recited in claim 19, further comprising:

a fourth linear gate structure having side surfaces oriented in the first direction and a top surface, wherein a width of the fourth linear gate structure is defined by a distance

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extending in the second direction between the side surfaces of the fourth linear gate structure, the width of the fourth linear gate structure substantially equal to the width of each of the first, second, and third linear gate structures, the fourth linear gate structure forming a gate electrode of at least one transistor,

wherein the first, second, third, and fourth linear gate structures are positioned in accordance with the substantially equal centerline-to-centerline pitch as measured in the second direction; and

a third gate contact in physical contact with the top surface of the fourth linear gate structure, the third gate contact formed to cover the width of the fourth linear gate structure without extending in the second direction substantially beyond either of the side surfaces of the fourth linear gate structure.

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